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| **Course Name:** | **Digital Design Laboratory** | **Semester:** | **III** |
| **Date of Performance:** | **\_\_\_ / \_\_\_ / \_\_\_\_\_\_** | **Batch No:** | **B4** |
| **Faculty Name:** |  | **Roll No:** | **16010122221** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_/25** |

**Experiment No: 3**

**Title: 4:1 Multiplexer and 3: 8 Decoder**

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| **Aim and Objective of the Experiment:** |
| To design and implement a 4:1 multiplexer and 3: 8 Decoder |

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| **COs to be achieved:** |
| **CO2**: Use different minimization techniques and solve combinational circuits. |

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| **Tools used:** |
| Trainer kits |

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| **Theory:** |
| **Multiplexer:** Multiplexer is a special type of combinational circuit. It is a digital circuit that selects one of the n data inputs and routes it to the output. The selection of one of the n inputs is done by the select lines. To select n inputs we require m select lines, such that 2m=n. Depending on the digital code applied at the select inputs, one out of the n data sources is selected and transmitted to a single output.  **Decoder:** A decoder is a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. The input code generally has fewer bits than the output code, and there is a one-to-one mapping from input code words into output code words. The general structure of a decoder circuit is shown in the Figure below. The enable inputs, if present, must be asserted for the decoder to perform its normal mapping function. The most commonly used input code is an N-bit binary code, where an N-bit word represents one of 2N different coded values. Normally, they range from 0 through 2N − 1. The input code lines select which output is active. The remaining output lines are disabled.  **Implementation Details:**  **4:1 Multiplexer Block Diagram**    **4:1 Multiplexer Circuit**    **Pin Diagram IC74153**  Analysis of a 4-Way Integrated Multiplexer ; the 74153 - Demultiplexers  **Implementation Details:**  **3:8 Decoder Block Diagram**    **3:8 Decoder Circuit**    **Pin Diagram IC74138**  74LS138 IC: Pin Configuration, Features, Circuit Diagram and Applications |

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| **Implementation Details** |
| **Procedure:**   1. Locate the IC 74153 and place the IC on trainer kit. 2. Connect VCC and ground to respective pins of IC trainer kit. 3. Implement the circuit as shown in the circuit diagram. 4. Connect the inputs to the input switches in the trainer kit. 5. Connect the outputs to the O/P LEDs 6. Apply various combinations of inputs according to the truth table and observe the condition of the LEDs. 7. Note down the corresponding output readings for various combinations of inputs. 8. Repeat the same for IC 74138 |
| **Post Lab Subjective/Objective type Questions:** |
| 1. Design and verify a 2:1 multiplexer using logic gates.   ANS1) **a. Prepare the function table of the 2:1 Mux:**  IMG_256  **b. Formulate the expression for output Y by considering only those FPs for which the output is 1. Y = S0’. D0 + S0 . D1 The simplified function can be tabulated as:**  IMG_257  **c. Draw the logic diagram for the expression:**  IMG_258  **d. Using simulator construct the circuit and verify its operation.**  **e. The same circuit can also be designed by having an active low enable input as shown in image. The simplified function can be tabulated as:**  IMG_259  IMG_260  **1.3. Encoder Logic** The figure shows the concept of encoder wherein input line 4 is high and all other inputs are low. The output of the encoder is a decimal 4, whose equivalent binary is 0100. The concept of decimal to binary(10 to 4 binary) encoder is shown in the figure given below. On similar lines an octal-binary encoder will have eight inputs and produce 3-bit binary output.  IMG_261   1. Build an 8:1 multiplexer using only 2:1 multiplexers.   ANS2) A multiplexer (MUX) is a digital circuit that selects one of several input signals and forwards it to a single output. An 8:1 multiplexer can be built using 2:1 multiplexers in a hierarchical manner. Here's how you can construct an 8:1 multiplexer using only 2:1 multiplexers: Inputs: A, B, C, D, E, F, G, H (8 input signals) S2, S1, S0 (3 select lines) Outputs: Y (Output signal)  In this diagram, each "M" block represents a 2:1 multiplexer. The inputs A, B, C, etc., are connected to the data inputs of the 2:1 multiplexers. The select lines S2, S1, and S0 are used to control the multiplexers' selection of input. Here's how you would connect the inputs and select lines to achieve an 8:1 multiplexer: Connect A, B, C, D, E, F, G, and H to the data inputs of the first set of 2:1 multiplexers.  Connect S2 to the select line of the first set of multiplexers. Connect the outputs of the first set of multiplexers to the data inputs of the second set of multiplexers.  Connect S1 to the select line of the second set of multiplexers. Connect the outputs of the second set of multiplexers to the data inputs of the third set of multiplexers. Connect S0 to the select line of the third set of multiplexers.  The output Y will be the output of the third set of multiplexers.  By controlling the select lines S2, S1, and S0, you can choose which input signal is forwarded to the output Y. This hierarchical arrangement allows you to build an 8:1 multiplexer using only 2:1 multiplexers. |

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| **Conclusion:** |
| We understood the concept of multiplexers and demultiplexers and implemented the same. |

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| **Signature of faculty in-charge with Date:** |